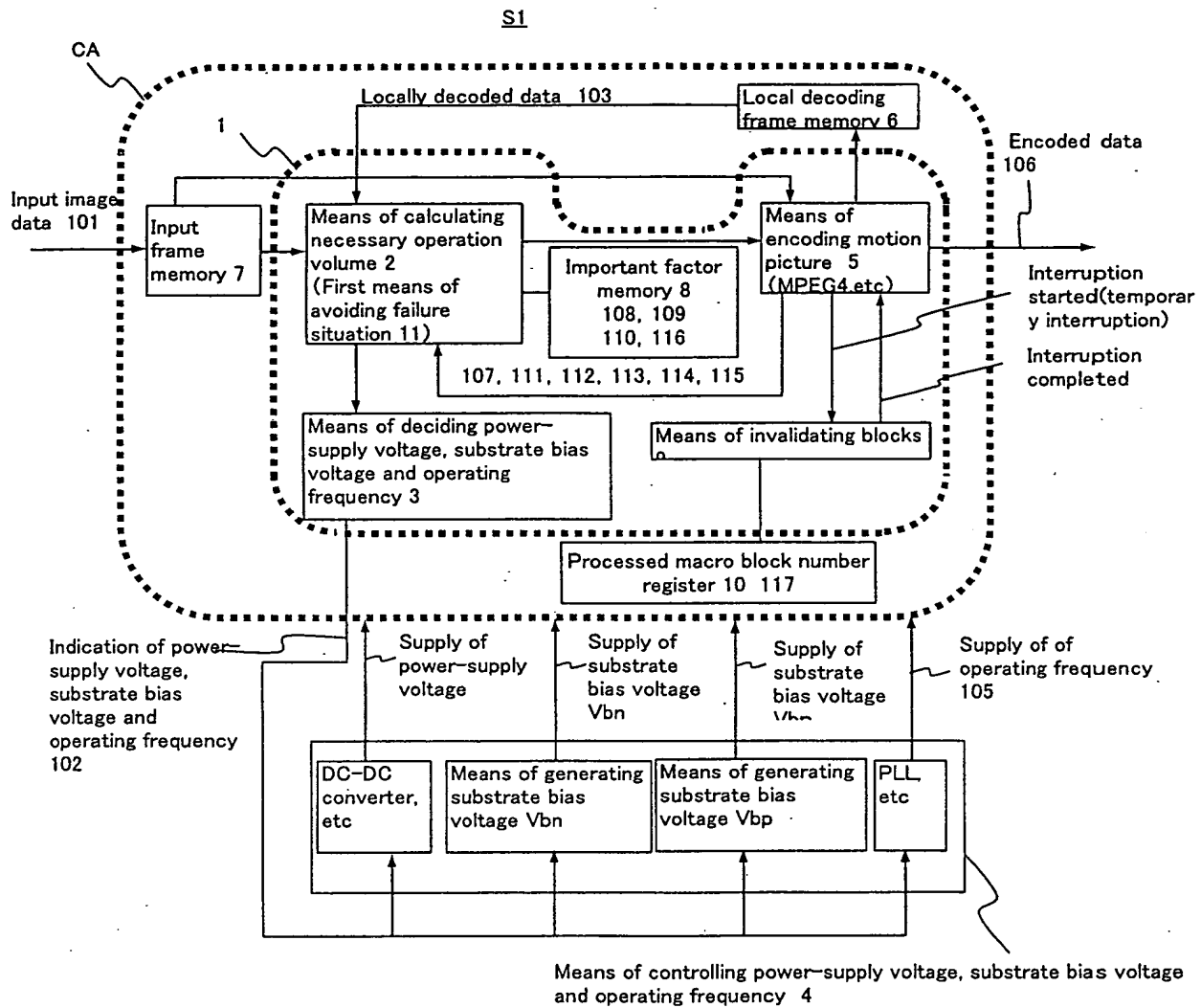
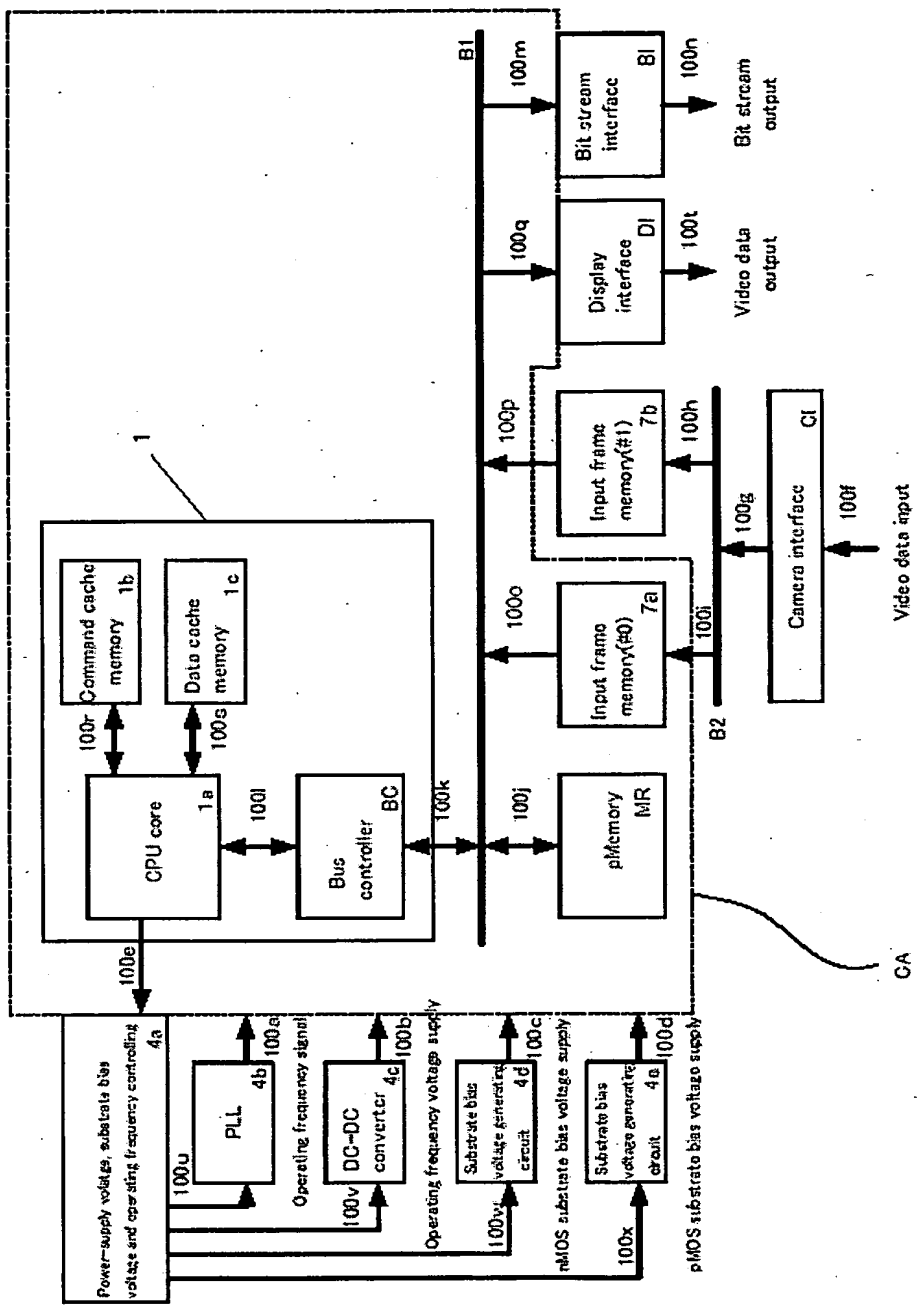


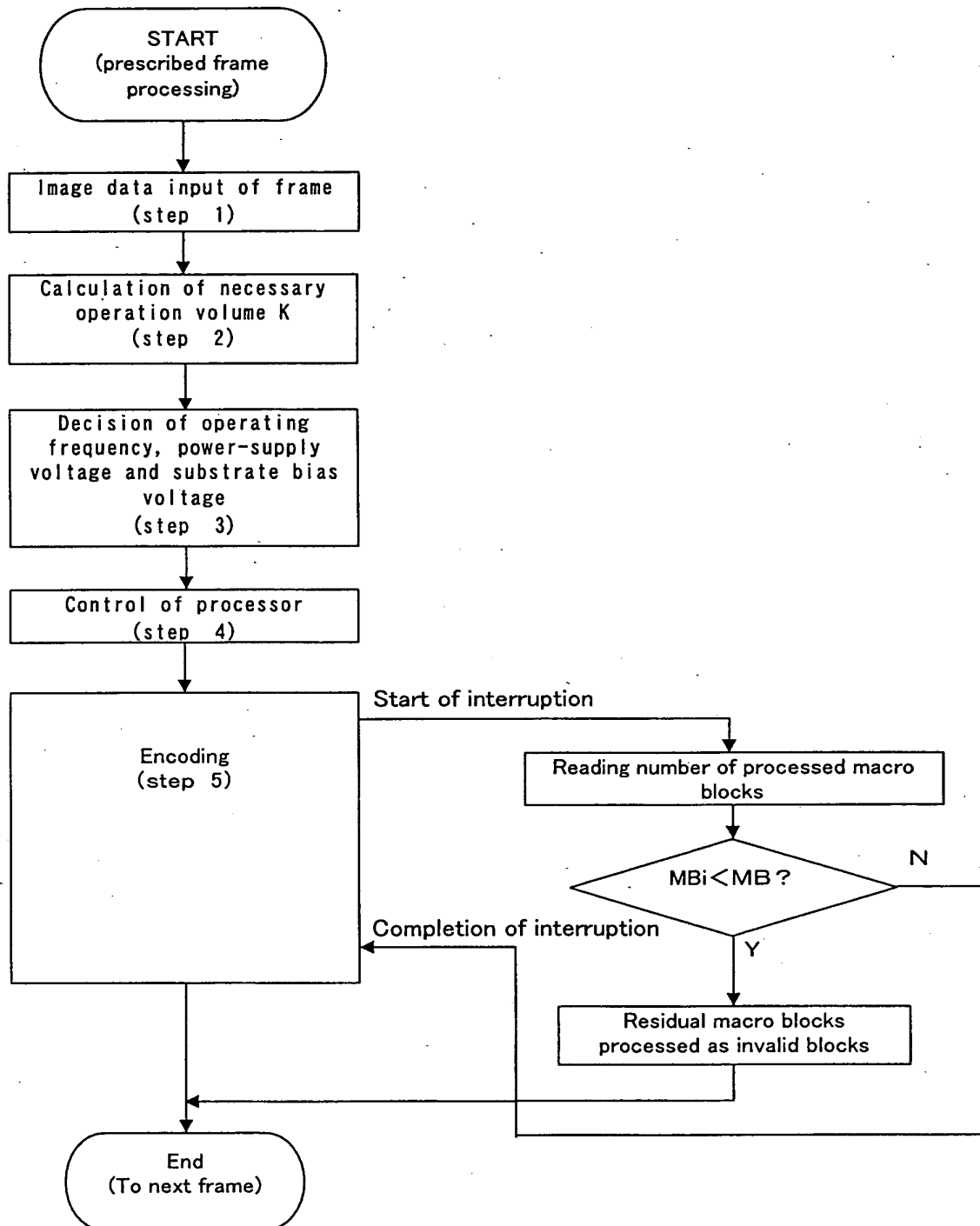
【Fig1】



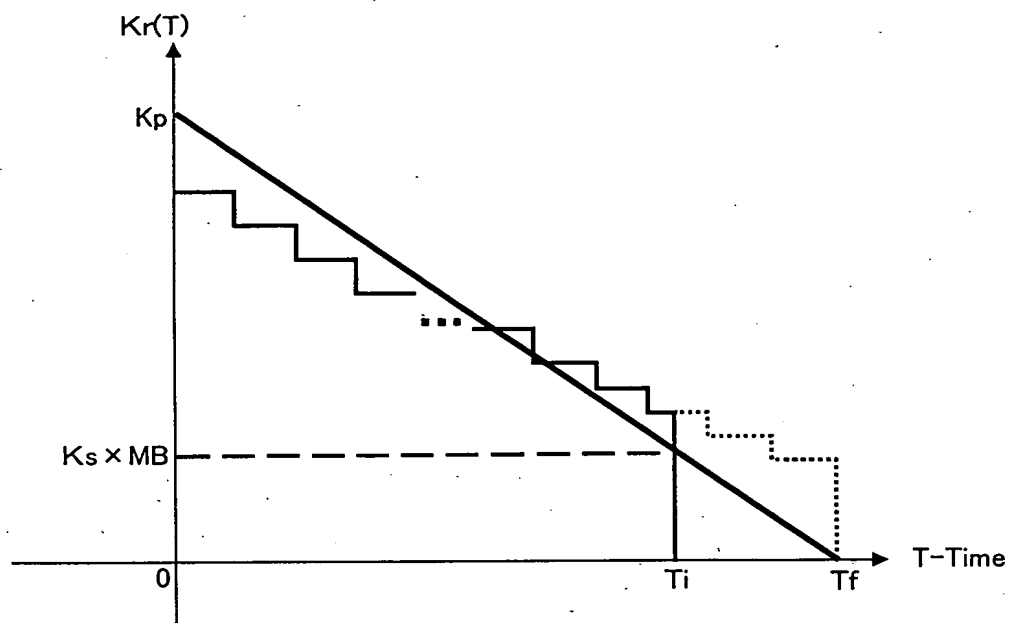
【Fig2】



【Fig3】



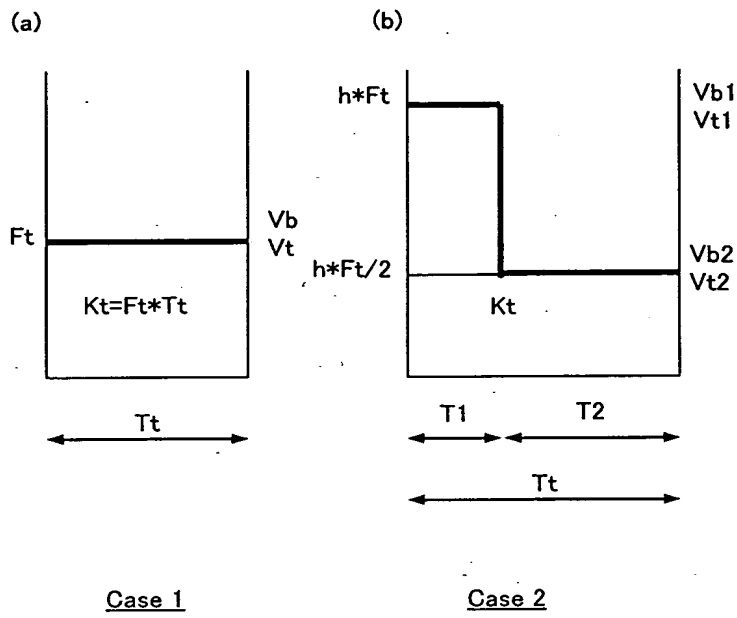
【Fig4】



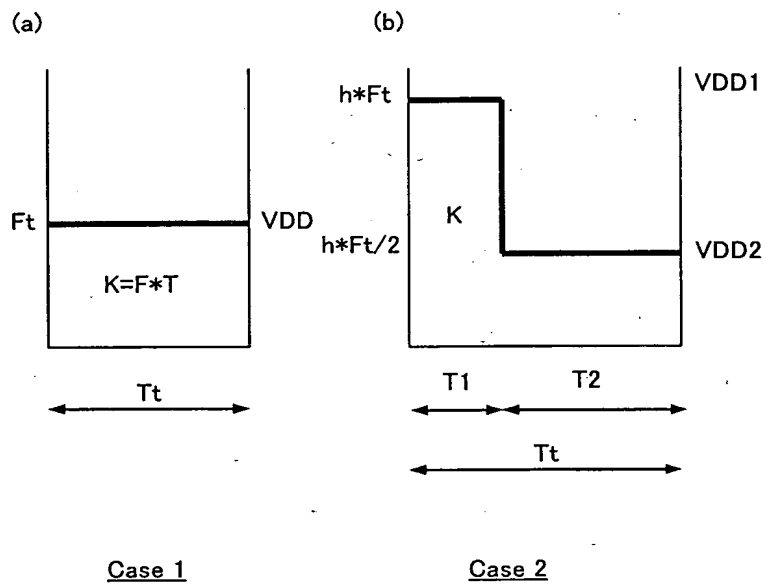
【Fig5】

Operating frequency (cycles/second)	Power-supply voltage (V DD)	Substrate bias voltage of n-channel MOS transistor (Vbn)	Substrate bias voltage of p-channel MOS transistor (Vbp)
f (1)	VDD (1)	Vbn (1)	Vbp (1)
f (2) (>f (1))	VDD (2)	Vbn (2)	Vbp (2)
f (3) (>f (2))	VDD (3)	Vbn (3)	Vbp (3)
.	.	.	.
f (n) (>f (n-1))	VDD (n)	Vbn (n)	Vbp (n)
.	.	.	.
f (r) (>f (r-1))	VDD (r)	Vbn (r)	Vbp (r)

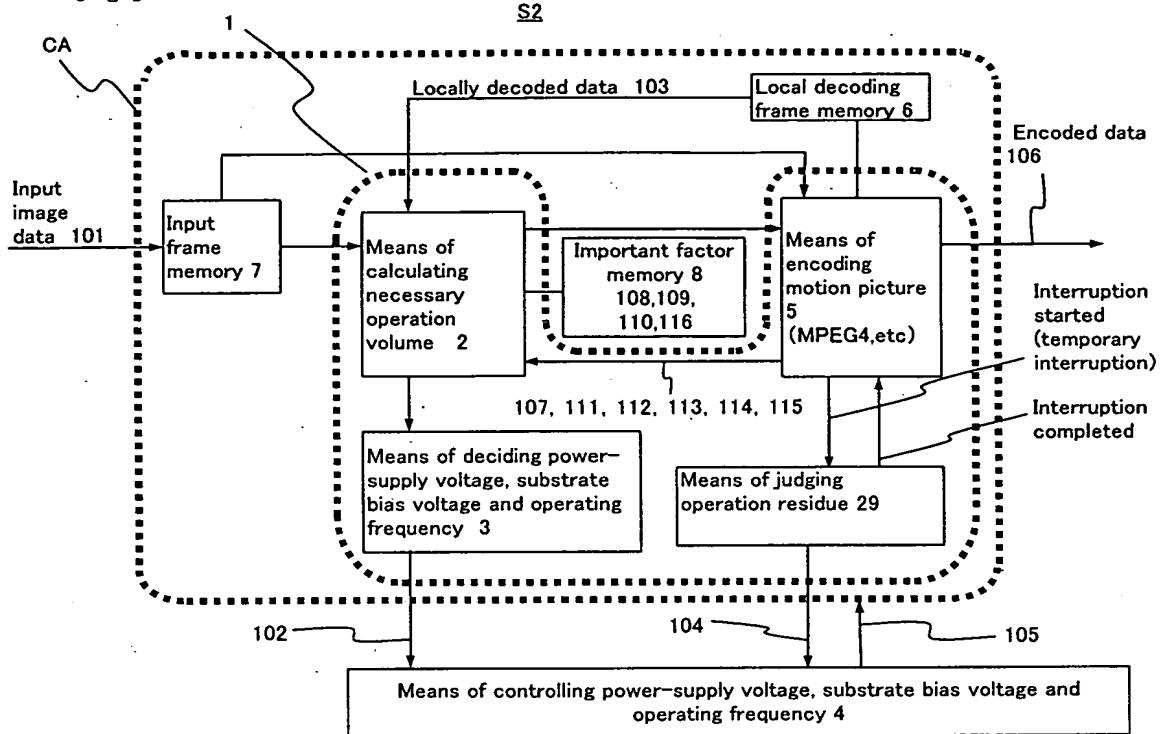
【Fig6】



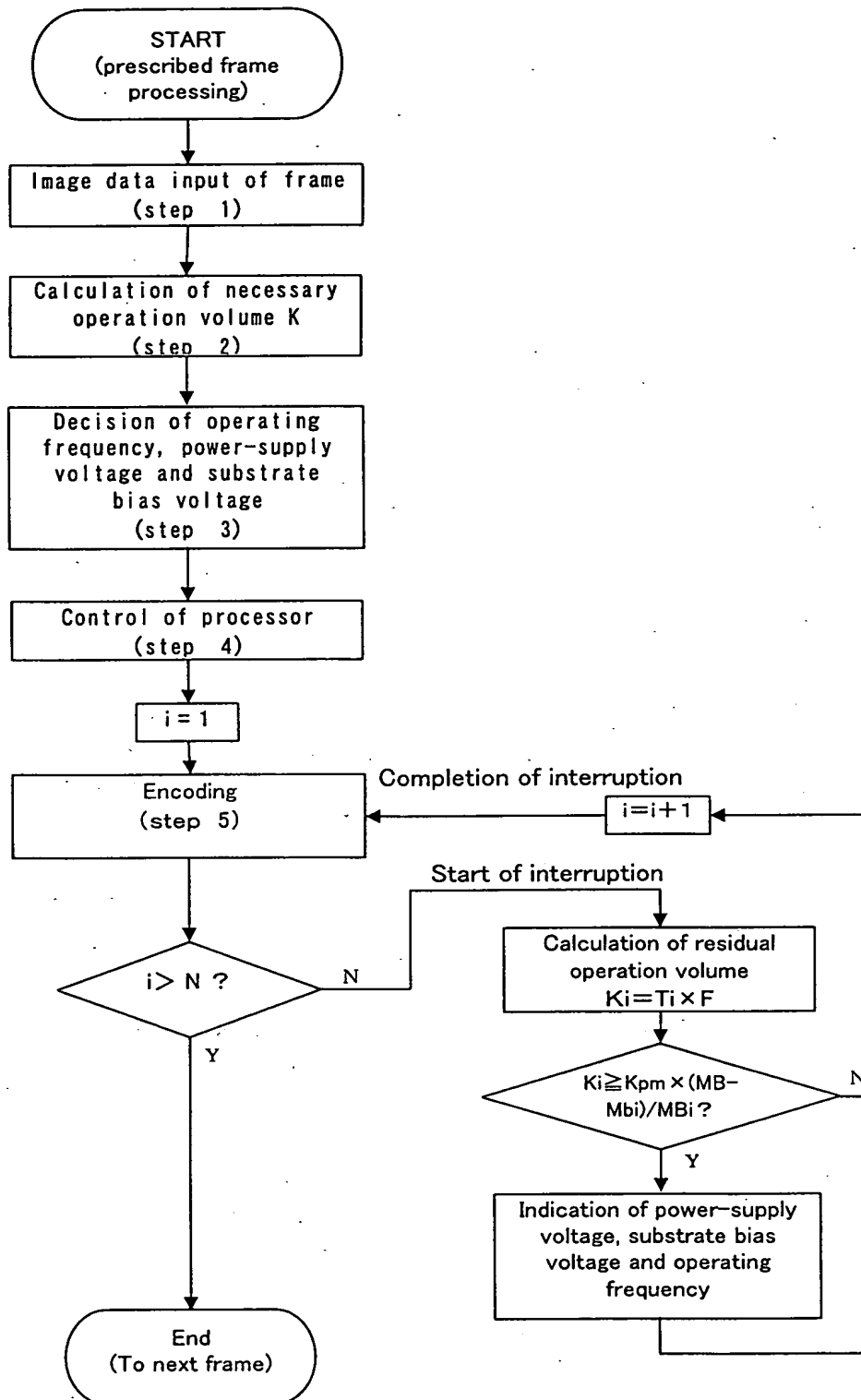
【Fig7】



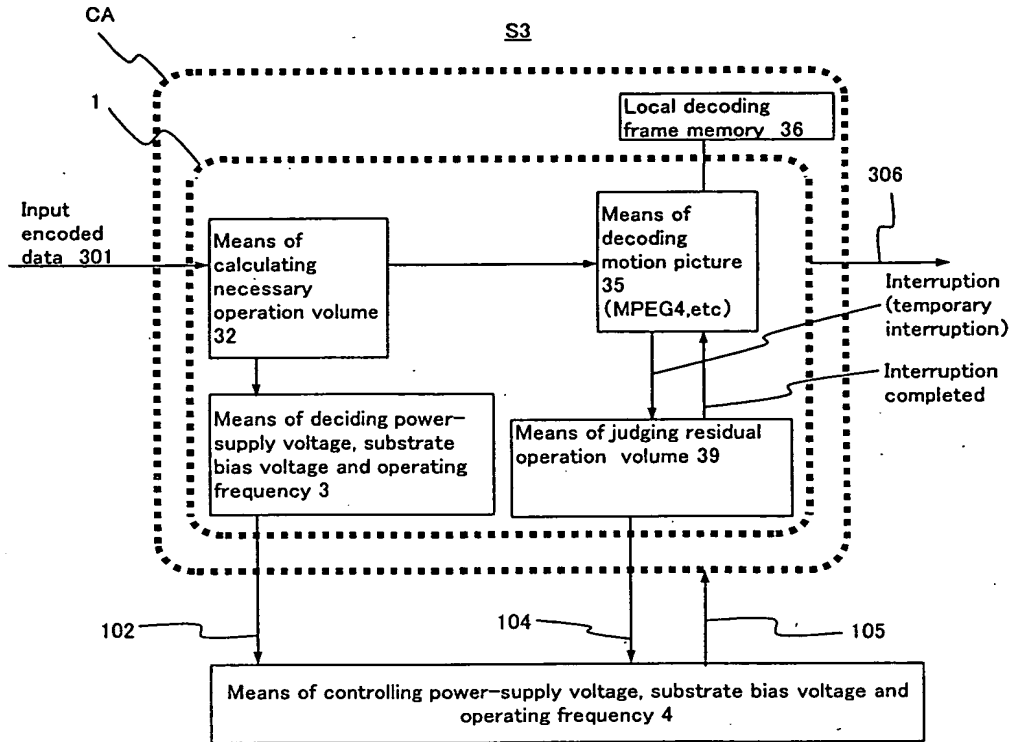
【Fig8】



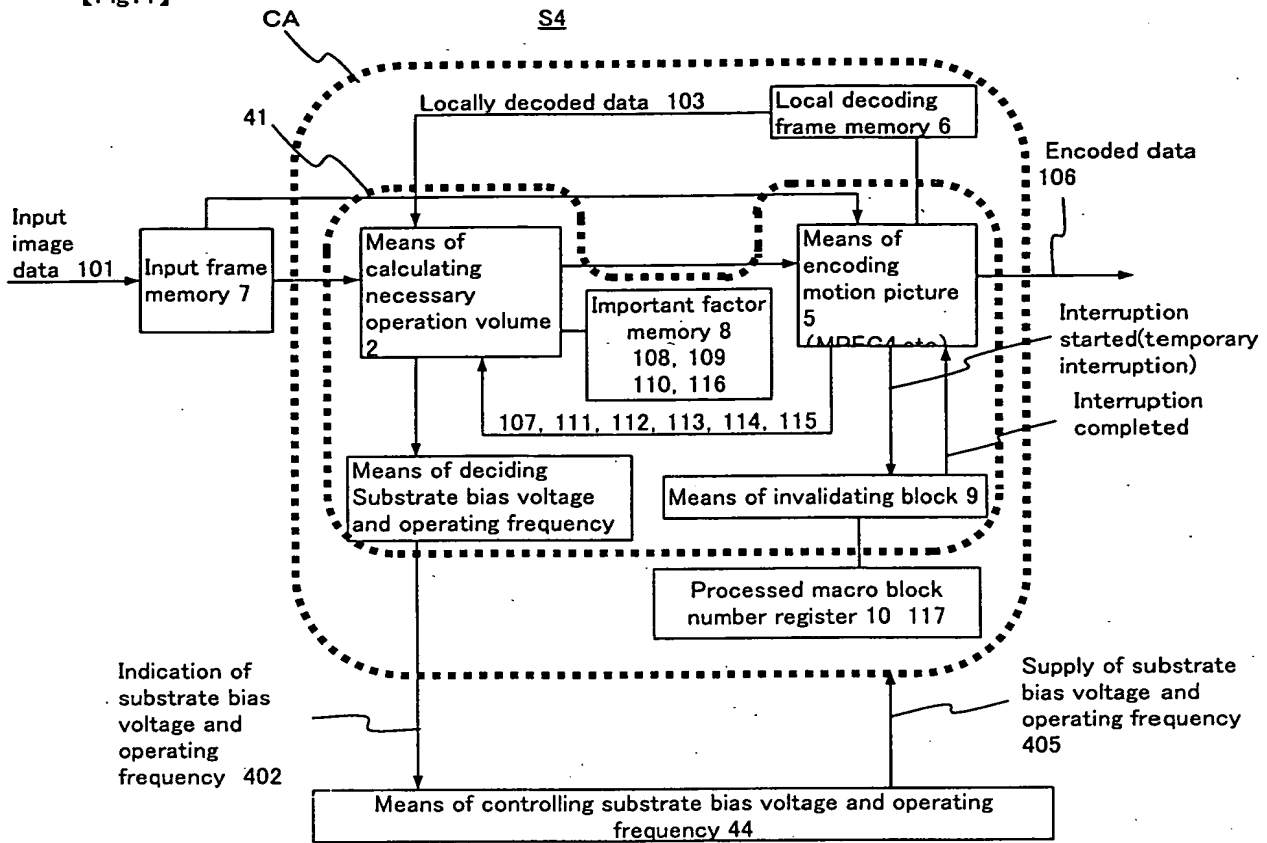
【Fig9】



[Fig10]



【Fig11】



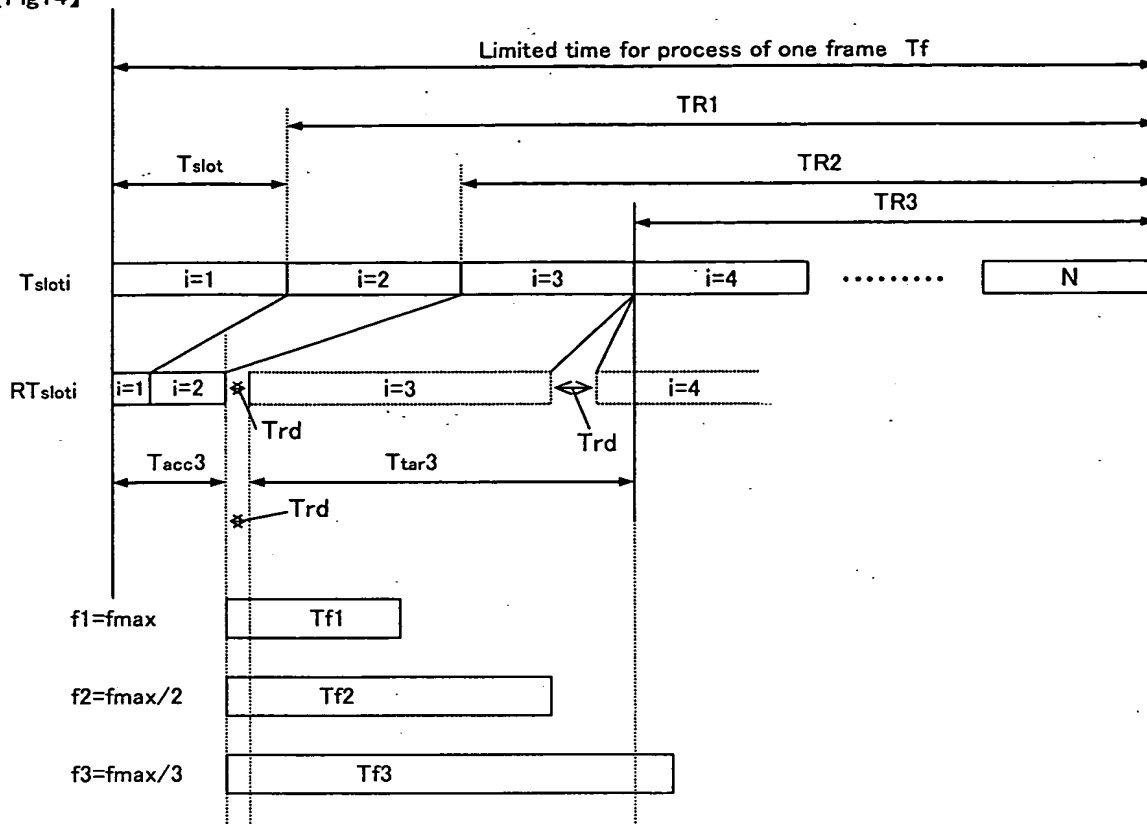
【Fig12】

Operating frequency (cycles/second)	Substrate bias voltage of n-channel MOS transistor (Vbn)	Substrate bias voltage of p-channel MOS transistor (Vbp)
f (1)	Vbn (1)	Vbp (1)
f (2) (>f (1))	Vbn (2)	Vbp (2)
f (3) (>f (2))	Vbn (3)	Vbp (3)
.	.	.
f (n) (>f (n-1))	Vbn (n)	Vbp (n)
.	.	.
f (r) (>f (r-1))	Vbn (r)	Vbp (r)

【Fig13】

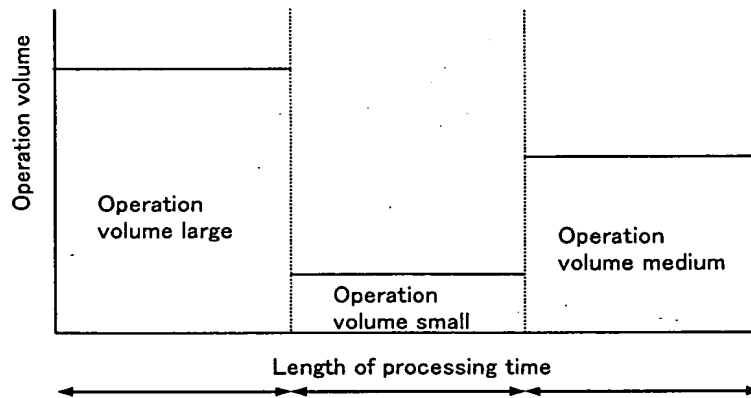
Operating frequency (cycles/second)	Power-supply voltage (VDD)	Substrate bias voltage of n-channel MOS transistor (Vbn)	Substrate bias voltage of p-channel MOS transistor (Vbp)
f (1)=50	VDD(1)=0.5	Vbn (1) = -1.0	Vbp (1) = 1.5
f (2)=100	VDD(2)=0.6	Vbn (2) = -0.4	Vbp (2) = 1.0
f (3)=150	VDD(3)=0.8	Vbn (3) = 0	Vbp (3) = 0.8
f (4)=200	VDD(4)=0.9	Vbn (4) = 0.2	Vbp (4) = 0.7
f (5)=250	VDD(5)=1.0	Vbn (5) = 0.5	Vbp (5) = 0.5

【Fig14】

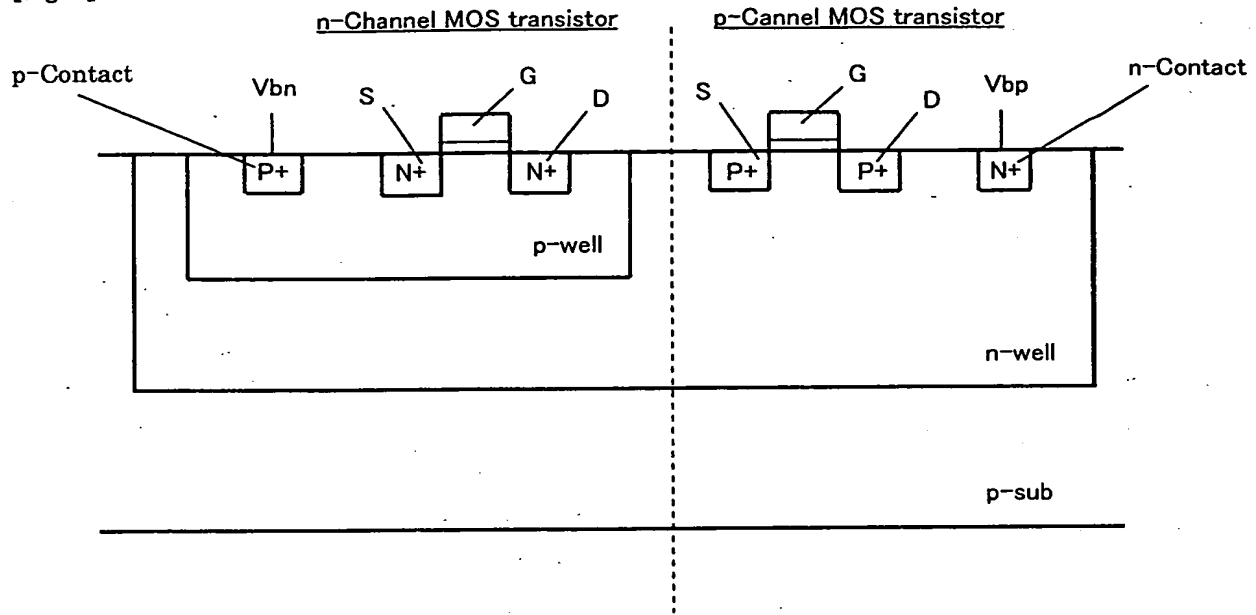


⇒ Operating frequency $F2$ is selected for time slot 3

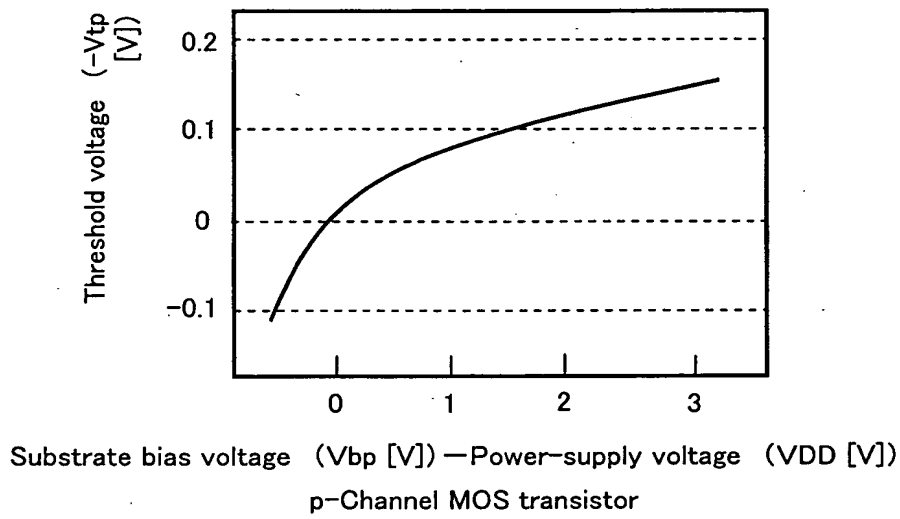
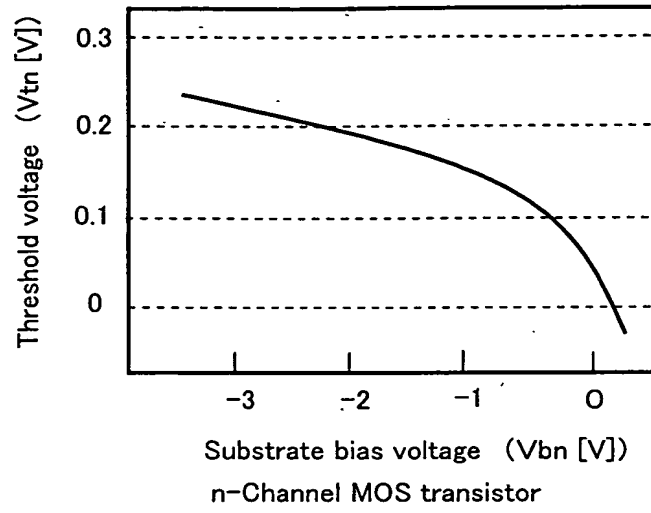
【Fig15】



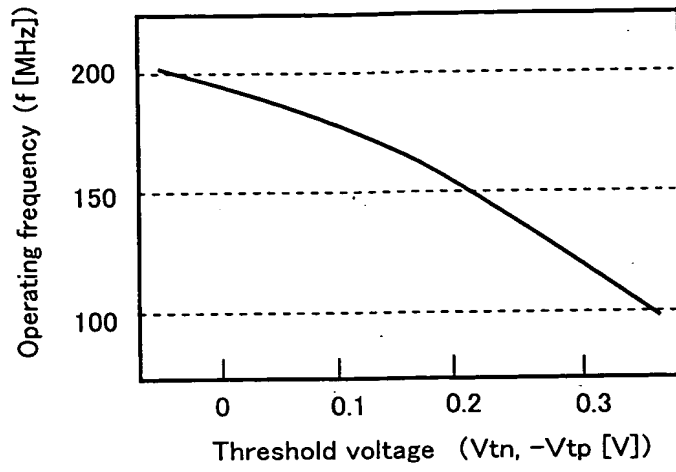
【Fig16】



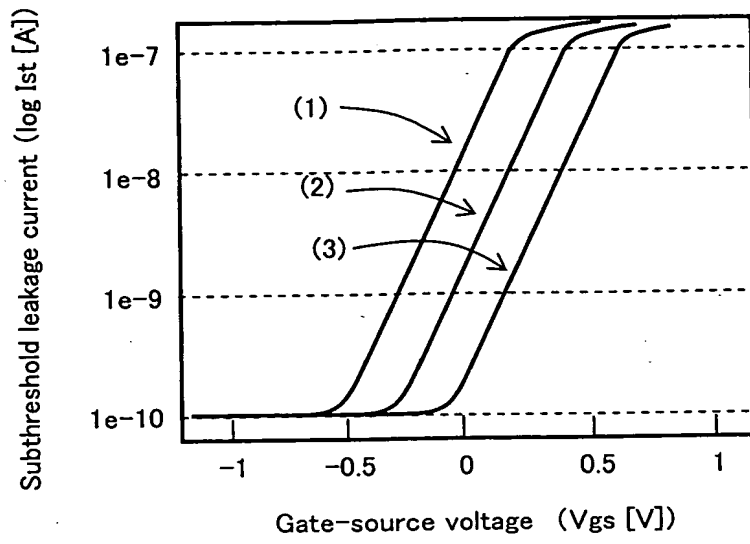
【Fig17】



【Fig18】



【Fig19】



【Fig20】

